IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1   1-28.   (Canceled)

1   29.   (Currently Amended) A program storage device readable by a computer,

2   the program storage device tangibly embodying one or more programs of instructions

3   executable by the computer to perform operations for determining when to perform an

4   error recovery instruction, the operations comprising:

5   receiving an error recovery instruction;

6   beginning a timeout task;

7   monitoring a processor interface to identify processor status for determining a

8   time to perform the error recovery instruction for withholding access to [[the]] a local

9   processor; and

10   performing the error recovery instruction when the monitoring determines a

11   time for performing the error recovery instruction.

1   30.   (Previously Presented)   The program storage device of claim 28

2   further comprising forcing an execution of the error recovery instruction when the

3   timeout task expires before the monitoring determines a time to perform the error

4   recovery instruction.

1   31.   (Previously Presented)   The program storage device of claim 30

2   further comprising resuming normal operations after performing the error recovery

3   instruction.

1   32.   (Previously Presented)   The program storage device of claim 28,

2   wherein the monitoring a processor interface to identify processor status for

3   determining a time to perform the error recovery instruction for withholding access to

4   the local processor further comprises:

5   monitoring a processor interface to a host bus for an idle condition;

6   withholding access to the processor interface when the idle condition is

7   detected;

8   after access to the processor interface is withheld, interrogating all data transfer

9   paths to determine when all the data paths are idle; and

10   identifying the time to perform the error recovery instruction when all data

11   transfer paths are idle.

1   33.   (Previously Presented)   The program storage device of claim 32

2   further comprising resuming normal operations after performing the error recovery

3   instruction.

1   34.   (Previously Presented)   The program storage device of claim 28

2   further comprising resuming normal operations after performing the error recovery

3   instruction.

1   35.   (Currently Amended) A program storage device readable by a computer,

2   the program storage device tangibly embodying one or more programs of instructions

3   executable by the computer to perform operations for determining when to perform an

4   error recovery instruction, the operations comprising:

5   receiving an error recovery instruction;

6   monitoring a processor interface to identify processor status for determining a

7   time to perform the error recovery instruction for withholding access to [[the]] a local

8   processor; and

9   performing the error recovery instruction when the monitoring determines a

10   time for performing the error recovery instruction.

1   36.   (Previously Presented)   The program storage device of claim 35

2   further comprising beginning a timeout task after receiving the error recovery

3   instruction and forcing an execution of the error recovery instruction when the timeout

4   task expires before the monitoring determines a time to perform the error recovery

5   instruction.

1   37.   (Previously Presented)   The program storage device of claim 36

2   further comprising resuming normal operations after performing the error recovery

3   instruction.

1   38.   (Previously Presented)   The program storage device of claim 35,

2   wherein the monitoring a processor interface to identify processor status for

3   determining a time to perform the error recovery instruction for withholding access to

4   the local processor further comprises:

5   monitoring a processor interface to a host bus for an idle condition;

6   withholding access to the processor interface when the idle condition is

7   detected;

8   after access to the processor interface is withheld, interrogating all data transfer

9   paths to determine when all the data paths are idle; and

10   identifying the time to perform the error recovery instruction when all data

11   transfer paths are idle.

1   39.   (Previously Presented)   The program storage device of claim 38

2   further comprising resuming normal operations after performing the error recovery

3   instruction.

1   40.   (Previously Presented)   The program storage device of claim 35

2   further comprising resuming normal operations after performing the error recovery

3   instruction.

1 41. (Currently Amended) An apparatus for quiescing processor control logic

2 upon receipt of an error recovery instruction, comprising:

3   self-quiesce logic for receiving an error recovery instruction; and

4   a timer, coupled to the self-quiesce logic, for determining when to force

5 execution of the error recovery instruction;

6   wherein the self-quiesce logic initiates the timer when the error recovery

7 instruction is received, begins to monitor a processor interface to identify processor

8 status for determining a time to perform the error recovery instruction for withholding

9 access to [[the]] a local processor and performs the error recovery instruction when

10 the monitoring determines a time for performing the error recovery instruction.

1 42. (Previously Presented)   The apparatus of claim 41, wherein the

2 self-quiesce logic forces an execution of the error recovery instruction when the timer

3 expires before the self-quiesce logic determines a time to perform the error recovery

4 instruction.

1 43. (Previously Presented)   The apparatus of claim 42, wherein the

2 self-quiesce logic allows resuming normal operations after the error recovery

3 instruction is performed.

1   44.   (Previously Presented)   The apparatus of claim 41, wherein the

2   self-quiesce logic monitors a processor interface to a host bus to identify processor

3   status for determining a time to perform the error recovery instruction for withholding

4   access to the local processor by monitoring the processor interface for an idle condition,

5   withholding access to the processor interface when the idle condition is detected, after

6   access to the processor interface is withheld, interrogating all data transfer paths to

7   determine when all the data paths are idle and identifying the time to perform the error

8   recovery instruction when all data transfer paths are idle.

1   45.   (Previously Presented)   The apparatus of claim 44, wherein the

2   self-quiesce logic allows resuming normal operations after the error recovery

3   instruction is performed.

1   46.   (Previously Presented)   The apparatus of claim 41, wherein the

2   self-quiesce logic allows resuming normal operations after the error recovery

3   instruction is performed.

1   47.   (Currently Amended) An apparatus for quiescing processor control logic

2   upon receipt of an error recovery instruction, comprising:

3   a processor for executing instructions; and

4   self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an

5   error recovery instruction, wherein the self-quiesce logic monitors a processor interface

6   to identify processor status for determining a time to perform the error recovery

7   instruction for withholding access to [[the]] a local processor and performs the error

8   recovery instruction when the monitoring determines a time for performing the error

9   recovery instruction.

1   48.   (Previously Presented)   The apparatus of claim 47 further

2   comprising a timer for determining when to abort the monitoring of processor status

3   and data path activity and cause an execution of the error recovery instruction.

1   49.   (Previously Presented)   The apparatus of claim 48, wherein the

2   self-quiesce logic causes normal operations to be resumed after performing the error

3   recovery instruction.

1   50. (Previously Presented) The apparatus of claim 47, wherein the

2 self-quiesce logic monitors a processor interface to a host bus to identify processor

3 status for determining a time to perform the error recovery instruction for withholding

4 access to the local processor by monitoring the processor interface for an idle condition,

5 withholding access to the processor interface when the idle condition is detected, after

6 access to the processor interface is withheld, interrogating all data transfer paths to

7 determine when all the data paths are idle and identifying the time to perform the error

8 recovery instruction when all data transfer paths are idle.

1   51. (Previously Presented) The apparatus of claim 50, wherein the

2 self-quiesce logic causes normal operations to be resumed after performing the error

3 recovery instruction.

1   52. (Previously Presented) The apparatus of claim 47, wherein the

2 self-quiesce logic causes normal operations to be resumed after performing the error

3 recovery instruction.

1   53.   (Currently Amended) A method for determining when to perform an

2   error recovery instruction, comprising:

3   receiving an error recovery instruction;

4   beginning a timeout task;

5   monitoring a processor interface to identify processor status for determining a

6   time to perform the error recovery instruction for withholding access to [[the]] a local

7   processor; and

8   performing the error recovery instruction when the monitoring determines a

9   time for performing the error recovery instruction.

1   54.   (Currently Amended) A method for determining when to perform an

2   error recovery instruction, comprising:

3   receiving an error recovery instruction;

4   monitoring a processor interface to identify processor status for determining a

5   time to perform the error recovery instruction for withholding access to [[the]] a local

6   processor; and

7   performing the error recovery instruction when the monitoring determines a

8   time for performing the error recovery instruction.

1   55.   (Currently Amended) An apparatus for quiescing processor control logic

2   upon receipt of an error recovery instruction, comprising:

3   means for receiving an error recovery instruction; and

4   means for determining when to force execution of the error recovery instruction;

5   wherein the means for receiving the error recovery instruction initiates a timer

6   when the error recovery instruction is received, begins to monitor a processor interface

7   to identify processor status for determining a time to perform the error recovery

8   instruction for withholding access to [[the]] a local processor and performs the error

9   recovery instruction when a time for performing the error recovery instruction is

10   determined.

1   56.   (Currently Amended) An apparatus for quiescing processor control logic

2   upon receipt of an error recovery instruction, comprising:

3   means for executing instructions; and

4   means, coupled to the means for executing instructions, for detecting an error

5   recovery instruction, monitoring a processor interface to identify processor status for

6   determining a time to perform the error recovery instruction for withholding access to

7   [[the]] a local processor and performing the error recovery instruction when a time for

8   performing the error recovery instruction is determined.